

Fast Solution of Linear and Quadratic Programs with an Analog Circuit

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Abstract—We present the design of an analog circuit which solves linear programming (LP) or Quadratic Programming (QP) problems. In particular, the steady-state circuit voltages are the components of the LP (QP) optimal solution. The proposed method is used to implement a LP-based Model Predictive Controller by using an analog circuit. VLSI design of an LP problem demonstrates nanosecond range solution latency. Simulative and experimental results show the effectiveness of the proposed approach.

I. INTRODUCTION

Analog circuits for solving optimization problems have been extensively studied in the past [1], [2], [3]. Our renewed interests stems from Model Predictive Control (MPC) [4]. In MPC at each sampling time, starting at the current state, an open-loop optimal control problem is solved over a finite horizon. The optimal command signal is applied to the process only during the following sampling interval. At the next time step a new optimal control problem based on new measurements of the state is solved over a shifted horizon. The optimal solution relies on a dynamic model of the process, respects input and output constraints, and minimizes a performance index. When the model is linear and the performance index is based on two-norm, one-norm or ∞ -norm, the resulting optimization problem can be cast as a linear program (LP) or a quadratic program (QP), where the state enters the right hand side (rhs) of the constraints.

We present the design of an analog circuit whose steady state voltages are the LP/QP optimizers. The proposed analog circuit can be used to repeatedly solve LPs or QPs with varying rhs and therefore is suited for linear or quadratic MPC controller implementation. For some classes of applications the suggested implementation can be faster, cheaper and consume less power than digital implementation. A comparison to existing literature reveals that the proposed circuit is simpler and faster than previously published designs.

The paper is organized as follows. Existing literature is discussed in Section II. For readability, a description of how to construct an analog circuit from a given LP [5] is presented in Section III. Section IV summarizes the equivalence between the LP and the circuit. Extensive treatment of LP properties and an extension to QP problems can be found in [5]. Section V presents an updated proof that the circuit is passive. The main novelty of this paper is a fast VLSI implementation that is shown in Section VI together with additional simulative and experimental results. Concluding remarks are presented in Section VII.

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II. PREVIOUS WORK ON ANALOG OPTIMIZATION

A. Optimization problems and electrical networks

Consider the linear programming (LP) problem

$$\min_{V=[V_1, \dots, V_n]} c^T V \quad (1a)$$

$$\text{s.t.} \quad A_{\text{eq}} V = b_{\text{eq}} \quad (1b)$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}} \quad (1c)$$

where $[V_1, \dots, V_n]$ are the optimization variables, A_{ineq} and A_{eq} are matrices, and c , b_{eq} and b_{ineq} are column vectors.

The monograph by J. Dennis [1] from 1959 presents an analog electrical network for solving the LP (1). In Dennis's work the primal and dual optimization variables are represented by the circuit currents and voltages, respectively. A basic version of Dennis's circuit consists of resistors, current sources, voltage sources and diodes. In this circuit each entry of matrices A_{ineq} and A_{eq} is equal to number of wires that are connected to a common node. Therefore, this circuit is limited to problems where the matrices A_{ineq} and A_{eq} contain only small integer values. An extended version of the circuit includes multiport DC-DC transformer and can represent arbitrary matrices A_{ineq} and A_{eq} . Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchoff's laws) are used to prove that the circuit converges to the solution of the optimization problem. This work had limited practical impact due to difficulties in implementing the circuit, and especially in implementing the multiport DC-DC transformer.

In later work, Chua [6] showed a different and more practical way to realize the multiport DC-DC transformer using operational amplifiers. In subsequent works, Chua [3], [7] and Hopefield [2] proposed circuits to solve non-linear optimization problem of the form

$$\begin{aligned} \min_x \quad & f(x) \\ \text{s.t.} \quad & g_j(x) \leq 0, \quad j = 1 \dots m \end{aligned} \quad (2)$$

where $x \in \mathbb{R}^n$ is vector of optimization variables, $f(x)$ is the cost function and $g_j(x)$ are the m constraint functions. The LP (1) was solved as a special case of problem (2) [3], [2]. The circuits proposed by Chua, Hopefield and coauthors model the Karush-Kuhn-Tucker (KKT) conditions by representing primal variables as capacitor voltages and dual variables as currents. The dual variables are driven by the inequality constraint violations using high gain amplifiers. The circuit is constructed in a way that capacitors are charged with a current proportional to the gradient of the Lagrangian

of problem (2)

$$\frac{\partial x_i}{\partial t} = - \left[\frac{\partial f(x)}{\partial x_i} + \sum_{j=1}^m I_j \frac{\partial g_j(x)}{\partial x_i} \right] \quad (3)$$

where $\frac{\partial x_i}{\partial t}$ is the capacitor voltage derivative and I_j is the current corresponding to the j -th dual variable. The derivatives $\frac{\partial f}{\partial x_i}$ and $\frac{\partial g_j}{\partial x_i}$ are implemented by using combinations of analog electrical devices [8]. When the circuit reaches an equilibrium, the capacitor charge is constant ($\frac{\partial x_i}{\partial t} = 0$) and equation (3) becomes one of the KKT conditions. The authors prove that their circuit always reaches an equilibrium point that satisfies the KKT conditions. This is an elegant approach since the circuit can be intuitively mapped to the KKT equations. However, the time required for the capacitors to reach an equilibrium is non-negligible. This might be the reason for relatively large settling time reported to be "tens of milliseconds" for those circuits in [3].

B. Applying analog circuits to MPC problems

The analog computing era declined before the widespread use of Model Predictive Control. Quero, Camacho and Franquelo in [9] have been the first to study the implementation of analog MPC. They use the Hopfield circuit proposed in [2] to implement an MPC controller. The approach they propose is validated with an experimental circuit which reaches the equilibrium after a transient of 1.8 msec.

More recently in [10] fast analog PI controllers are implemented on an Analog's Field Programmable Analog Array (FPAA) device [11] for an application involving fast chemical microreactor. The analog circuit designed in [10] has a computation time faster than a digital controller implementing the PI controller. The article briefly proposes to use FPAA for MPC without specifying details. To the best of authors knowledge, no further work has been published in this direction.

III. LP ANALOG CIRCUIT

Without loss of generality, we assume that A_{ineq} , A_{eq} and c have non-negative entries. Any LP (1) can be transformed into this form by introducing an auxiliary vector \bar{V} as follows:

$$\begin{aligned} \min_{\bar{V}, V} \quad & c^+ V + c^- \bar{V} \\ \text{s.t.} \quad & A_{\text{eq}}^+ V + A_{\text{eq}}^- \bar{V} = b_{\text{eq}}, \quad A_{\text{ineq}}^+ V + A_{\text{ineq}}^- \bar{V} \leq b_{\text{ineq}} \\ & V + \bar{V} = 0, \end{aligned}$$

where A_{ineq} , A_{eq} , and c are split into positive and negative parts ($A_{\text{ineq}} = A_{\text{ineq}}^+ - A_{\text{ineq}}^-$, $A_{\text{eq}} = A_{\text{eq}}^+ - A_{\text{eq}}^-$ and $c = c^+ - c^-$).

In the beginning of this section we present the basic building blocks which will be later used to create a circuit that solves problem (1). The first basic block enforces equality constraints of the form (1b). The second building

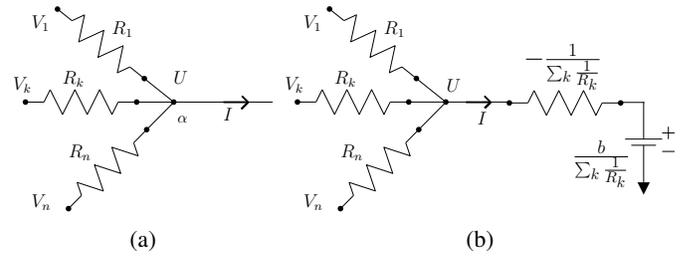


Fig. 1: (a) A node with k connected wires. (b) Equality enforcing circuit. Consists of n resistors R_k , a negative resistance and a reference voltage.

block enforces inequality constraints of the form (1c). The last basic block implements the cost function.

A. Equality constraint

Consider the circuit depicted in Fig. 1a. In this circuit n wires are connected to a common node. We call this common node α , its potential is U and the current that exits this node is I . Kirchhoff's current law (KCL) implies

$$\sum_{k=1}^n I_k = \sum_{k=1}^n \frac{V_k - U}{R_k} = I, \quad (5)$$

where V_k is the potential of node k , R_k is the resistance between node k and the node α . Equation (5) can be written as an equality constraint on potentials V_k :

$$\sum_{k=1}^n \frac{V_k}{R_k} = I + U \sum_{k=1}^n \frac{1}{R_k}. \quad (6)$$

If we can set the right hand side (rhs) of (6) to any desired value b , then (6) enforces an equality constraint on a linear combinations of V_k . Therefore every equality constraint (1b) can be implemented with a circuit which enforces (6) and implements

$$U = \frac{b - I}{\sum_{k=1}^n \frac{1}{R_k}}. \quad (7)$$

Equation (7) together with (6) yields

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = b. \quad (8)$$

and the circuit implementing (8) is shown in Fig. 1b.

Remark 1: In the circuit in Fig. 1b the negative resistance $-\frac{1}{\sum_k \frac{1}{R_k}}$ can be realized by using operational amplifier.

B. Inequality constraint

Consider the circuit shown in Fig. 2a. Similarly to the equality constraint circuit, n wires are connected to a common node α . Its potential is U and the current exiting this node is I . Kirchhoff's current law (KCL) implies (5).

An ideal diode connects node α to node β . The potential of node β is U' . The diode enforces $U \leq U'$. In Fig. 2a, the voltage U' can be computed as follows

$$U' = \frac{b - I}{\sum_{k=1}^n \frac{1}{R_k}} \geq U. \quad (9)$$

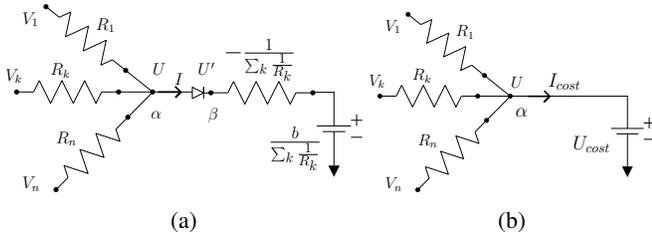


Fig. 2: (a) Inequality enforcing circuit. (b) Cost circuit.

Equation (5) and $U \leq U'$ yield

$$\sum_{k=1}^n \frac{V_k}{R_k} = I + U \sum_{k=1}^n \frac{1}{R_k} \leq I + U' \sum_{k=1}^n \frac{1}{R_k} = b. \quad (10)$$

Which can be compactly rewritten as

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \leq b. \quad (11)$$

C. Cost function

Consider the circuit in Fig. 2b. In this circuit the potential of node α is equal to U_{cost} and the current that exits the node is I_{cost} . From (6) we have

$$c^T V = I_{\text{cost}} + U_{\text{cost}} \sum_{k=1}^n \frac{1}{R_k} \triangleq J. \quad (12)$$

where $c = [1/R_1 \ \dots \ 1/R_n]$, $V = [V_1 \ \dots \ V_n]$ and J is the cost function.

This part of the circuit implements the minimization of the cost function. When U_{cost} is set to a low value, the voltages V_k are driven to a direction which forces the cost J to approach the U_{cost} value. However, the cost J is different from U_{cost} because the current I_{cost} is not zero. A detailed explanation on this part of the circuit can be found in [5].

D. Connecting the basic circuits

This section presents how to construct the circuit that solves a general LP. We construct the conductance matrix $G \in \mathbb{R}^{(m+1) \times n}$ as

$$G \triangleq \begin{bmatrix} c^T \\ A \end{bmatrix} = \begin{bmatrix} c^T \\ A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix} \quad (13)$$

and denote G_{ij} the i, j element of G . For a given LP (1) the R_{ij} resistor is defined as

$$R_{ij} = \frac{1}{G_{ij}}, \quad i = 0, \dots, m, \quad j = 1, \dots, n \quad (14)$$

where the first row of G (corresponding to c^T) is indexed by 0.

Consider the circuit shown in Fig. 3. The circuit is shown using a compact notation where each resistor R_{ij} is represented by a dot, vertical wires represent variables nodes with potentials $V_1 \dots V_n$ and horizontal wires represent *constraint nodes*. The compact representation of a resistor through the

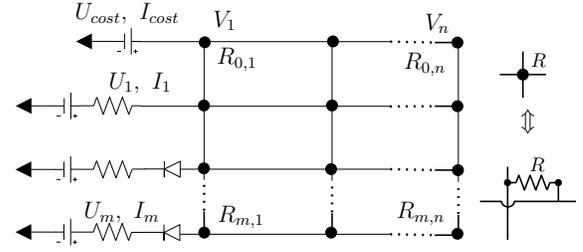


Fig. 3: Electric Circuit solving an LP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent resistances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Each horizontal wire is connected to a ground via a negative resistance, a constant voltage source and a diode for inequalities nodes. The topmost horizontal wire is the cost circuit which is connected to a constant voltage source.

dot symbol is clarified in Fig. 3. If $G_{ij} = 0$ then no resistor is present in the corresponding dot.

The LP circuit is constructed by connecting the nodes associated with the variables $V_1 \dots V_n$ to all three types of the basic circuits: equality, inequality and cost. We will refer to such nodes as *variable nodes*. Each row of the circuit in Fig. 3 is one of the basic circuits presented in Sections III-A, III-B and III-C. We claim that, if U_{cost} is “small enough”, then the values of the potentials $V_1 \dots V_n$ in this circuit are a solution of (1). This claim is proven in the next section.

Remark 2: The circuit as shown in Fig. 3 contains no dynamic elements such as capacitor or inductance. Therefore, the time required to reach steady-state is governed by the parasitic effects (e.g. wires inductance and capacitance) and by the properties of the elements used to realize negative resistance (usually opamp) and diode. Hence, a good electronic design can achieves solution times in the order of these parasitic effects. This could lead to time constants as low as a few nanoseconds.

IV. STEADY-STATE ANALYSIS OF THE LP CIRCUIT

Consider the LP circuit in Fig. 3 with R_{ij} defined by equations (13)-(14). In this section we show that there exists a range of U_{cost} values such that the LP circuit in Fig. 3 solves the optimization problem (1). In particular, the steady-state circuit voltages are the components of an LP optimal solution. First, we derive the steady state equations of the electric circuit and then we state an equivalence theorem.

A. Steady state solution

Consider the circuit in Fig. 3. Let $U = [U_1, \dots, U_m]^T$ be the voltages of the constraint nodes as shown on Fig. 3. By applying the KCL (Kirchhoff’s current law) we can show [5]

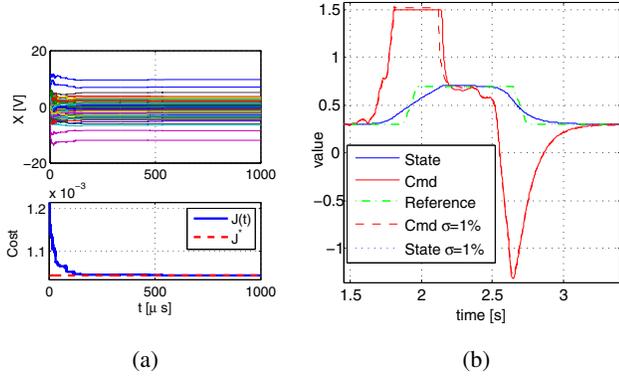


Fig. 5: (a) Example of LP solution. The upper plot shows solution variables and the lower shows the cost function value.(b)Example of MPC implementation. Solid lines represent nominal controller, dashed lines represent random 1% error of analog devices.

longer convergence time is not of practical interest, because the difference between the immediate cost value and the true optimal one is less than the accuracy that is expected from analog devices.

B. MPC example

This example demonstrates the implementation of a model predictive controller with an LP analog circuit. For this example we work with the dynamical system $\frac{dx}{dt} = -x + u$, where x is the system state and u is the input. We want x to follow a given reference trajectory, while satisfying input constraints. The finite time optimal control problem at time t is formulated as

$$\min_{u_0 \dots u_{n-1}} \sum_{i=1}^N |x(i) - x_{ref}(i)| \quad (16a)$$

$$x_{i+1} = x_i + (u_i - x_i)\delta, \quad i = 0, \dots, N \quad (16b)$$

$$-1.5 \leq u_i \leq 1.5, \quad i = 0, \dots, N \quad (16c)$$

$$x_0 = x(t) \quad (16d)$$

where N is the prediction horizon, $x_{ref}(i)$ is the reference trajectory at step i , δ is sampling time and $x(t)$ is the initial state at time t . Only the first input, u_0 , is applied at each time step t .

With $N = 16$, the LP in (16) has 96 variables, 63 equality constraints and 49 inequality constraints. An electric circuit that implements system dynamics together with the circuit that implements the MPC controller were constructed and simulated using SPICE. The voltage value representing the system state was measured and enforced on the x_0 node of the LP. The optimal input value u_0 was injected as input to the simulated system dynamics. Fig. 5b shows the closed loop simulations results. Notice the predictive behavior of the closed loop control input and the satisfaction of the system constraints.

In order to demonstrate system performance for imperfect analog devices, another simulation result with 1% random

TABLE I: Experimental and theoretical results (in parenthesis) for LP solution.

cost direction	x1 (exact)	x2 (exact)
1 1	4.996 (5.0)	4.99 (5.0)
-1 1	7.002 (7.0)	5.005 (5.0)
-1 -1	-7.012 (-7.0)	-4.98 (-5.0)
1 0	6.976 (7.0)	0.005 (0.0)

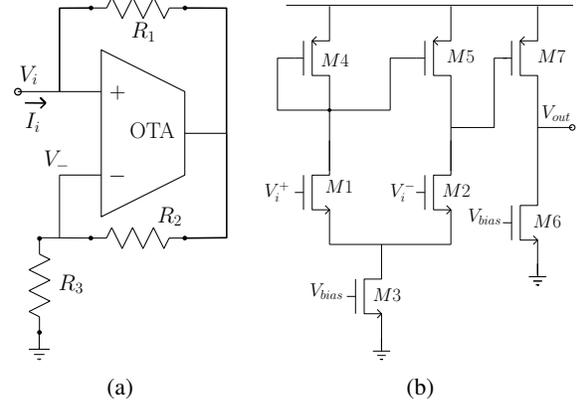


Fig. 6: (a) Implementation of a negative resistance with OTA, $V_i = -I_i R_1 R_3 / R_2$. (b) OTA implemented as two stage differential amplifier.

Gaussian error in values of resistors is presented on the same Fig. 5b. There is no significant change in system behavior.

C. Hardware implementation example

We implemented a small LP using standard electronics components. The same problem was realized by Hopfield [2] and Chua [3]. The LP is defined as follows

$$\begin{aligned} \min_{x_1, x_2} c^T [x_1 \ x_2]^T \\ \text{s.t. } 5x_1/12 - x_2 \leq 35/12, \quad 5x_1/2 + x_2 \leq 35/2 \\ -x_1 \leq 5, \quad x_2 \leq 5 \end{aligned} \quad (17)$$

where c is a cost vector, that is varied to get different solution points. The circuit was realized using resistors of 1% accuracy, operational amplifiers (OP27) for the negative resistance and comparator (LM311) together with the switch (DG201) to implement functionality of an ideal diode .

Various values for the cost function c and test results are summarized in Table I. Table I shows that the experimental results are accurate up to 0.5%. The circuit reaches an equilibrium 6 μs after the cost voltage was applied. The convergence time is governed by a slew rate of the OP27 that is limited to 2.8 V/ μs .

D. LP implementation on CMOS integrated circuit

We study the feasibility of constructing a high speed LP solver utilizing custom CMOS integrated circuit. In this work, amplifier, comparator, negative resistance and an ideal diode devices were developed using FreePDK45 library for 45nm CMOS and Cadence's CAD tools.

Implementation schematics of a negative resistance using Operational Transconductance Amplifier (OTA) and resistors

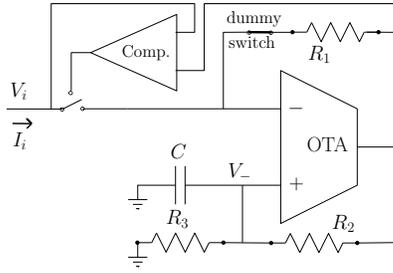


Fig. 7: Implementation of an ideal diode with switch and comparator.

is shown in Fig. 6a. The OTA was realized using a common topology of dual stage differential amplifier, as shown in Fig. 6b. The transistors $M1, M2, M4, M5, M6$ and $M7$ have size ($L \times W$) of $250nm \times 200nm$ for the first stage, and size of $250nm \times 1000nm$ for the second stage. The transistor $M3$ has size of $375nm \times 200nm$.

Fig. 7 shows an integrated implementation of an ideal diode and a negative resistance that realize an inequality circuit as in Fig. 2a. Ideal diode functionality is achieved with a comparator that drives a switch. The comparator closes the switch only when it senses a voltage difference that indicates a positive current I_i . The comparator is implemented using the same topology as the OTA (Fig. 6b) but with smaller device size ($L = 60nm$) that yields a higher bandwidth. A dummy switch and a capacitor C are added to compensate additional resistance and capacitance due to addition of the switch and the comparator.

From those building blocks a simple LP (18) was constructed and evaluated in simulation. Dynamic range from $400mV$ to $600mV$ was allocated for the variables, since the used technology has a maximum voltage of $1V$.

$$\begin{aligned} \min_{V_{out}, V_2, V_{in}} V_{out} \\ \text{s.t. } V_{out} + V_2 = 1, \quad V_{in}/3 + V_2/1.5 \leq 0.53, \quad V_{in} = V_{ext}, \end{aligned} \quad (18)$$

where $V_{ext} = 0.5 + 0.02 \sin(\omega t)$ with $\omega = 100$ MHz.

The designed LP circuit was tested with 100 MHz input signal. Output of a non-linear transient device-level simulation of the circuit is shown in Fig. 8. The input voltages V_{in} oscillates between roughly $0.52V$ to $0.48V$. In this case the inequality constraint is always active. From comparison to the exact solution, as shown in Fig. 8, the output voltage V_{out} has an error of $3 mV$ that is 1.5% of the dynamic range and is delayed by $5ns$.

VII. CONCLUSION

In this paper we presented an approach to design an electric analog circuit that is able to solve feasible Linear and Quadratic Programs. The method is used to implement and solve MPC based on linear programming. We present simulative and the experimental results that demonstrate the effectiveness of the proposed method.

The reported LP solution speed of $6 \mu s$ is faster than any result that was previously reported in the literature, and may be significantly decreased further by selecting

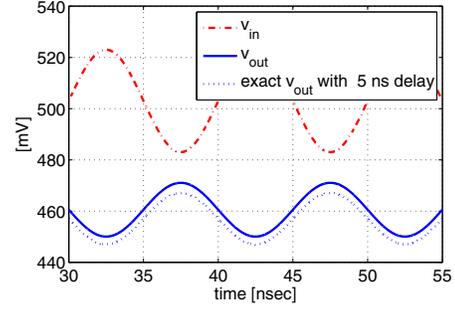


Fig. 8: Simulation results of CMOS circuit for LP (18).

faster components or implementing the design using faster technology, as was shown with the custom VLSI design.

Future research directions have interesting theoretical and implementations challenges. The theoretical aspects include analog complexity theory and the study the dynamic circuit behavior using the theory of Linear Complimentary system [12]. The implementations aspects includes solutions to the optimal circuit design, implementation using VLSI technologies and application to real-world problems.

VIII. ACKNOWLEDGMENTS

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